KA49703A
Application Notes

Battery Monitoring IC (BMIC)
for Industrial Application

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Contents

- Chapter 1 Overview 3
- Chapter 2 Input RC and components setting for Cell Balance operation 4
- Chapter 3 Regulators Components and setting 10
- Chapter 4 Unused pins setting 13
- Chapter 5 Battery Cell inputs connection sequence 15
- Chapter 6 Daisy Chain Connection 16
- Chapter 7 KA49703A as Communication IC Connection 20
- Chapter 8 16-Channels TMONI using Multiplexer 21
- Chapter 9 PCB Layout Guideline 23

Chapter 1 Overview

1.1 Description

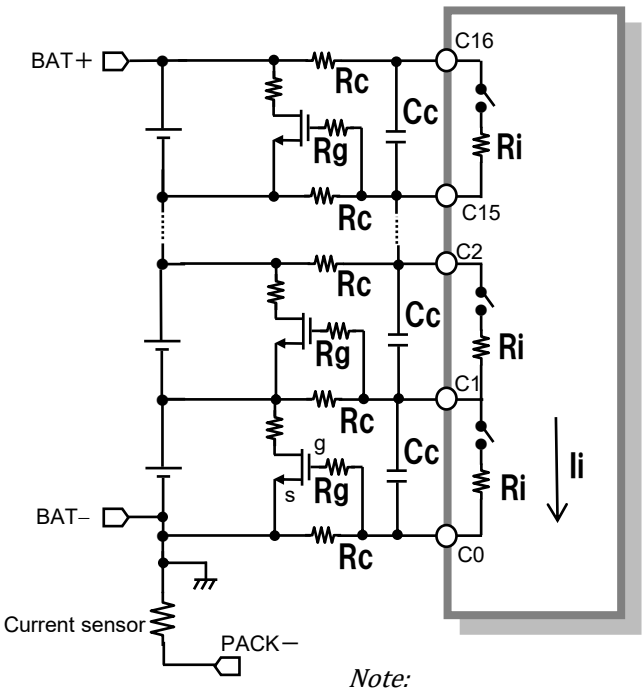
This is the application note for using KA49703A, which is a stackable battery monitoring IC with protection function.

All the materials in this application notes are provided as design references only and not mass production guaranteed.

Sufficient evaluation and verification is required prior to mass production.

Chapter 2 Input RC and components setting for Cell Balance operation

2.1 RC external Cell Balancing



Note:
Rg value recommended as 1kohm for hotplug solution

Fig. 2.1.1 Parameter for external cell balance

1) *Calculate Rc*

$$Vgs = \frac{Vcell * Rc}{2Rc + Ri} \qquad Ri = 20ohm$$

$Vgs \geq Vth(in\ order\ to\ turn\ on\ FET)$

$Suppose\ Vth = 1.5V$ Vcell = 3.7V

$$Rc \geq Ri * \frac{Vth}{Vcell - 2Vth} = 43ohm$$

$and\ Rc < 5kohm\ (for\ input\ impedance\ limitation)$

$Rc = 1kohm{\sim}4kohm\ is\ recommended$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$

$$\left(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us * 2} = 10kHz\right)$$

$eg.\ when\ fs = 20kHz, Rc = 1kohm$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.008\text{uF}$$

$Using\ 10 * Cc\ \ is\ recommended$

2.2 RC internal Cell Balancing

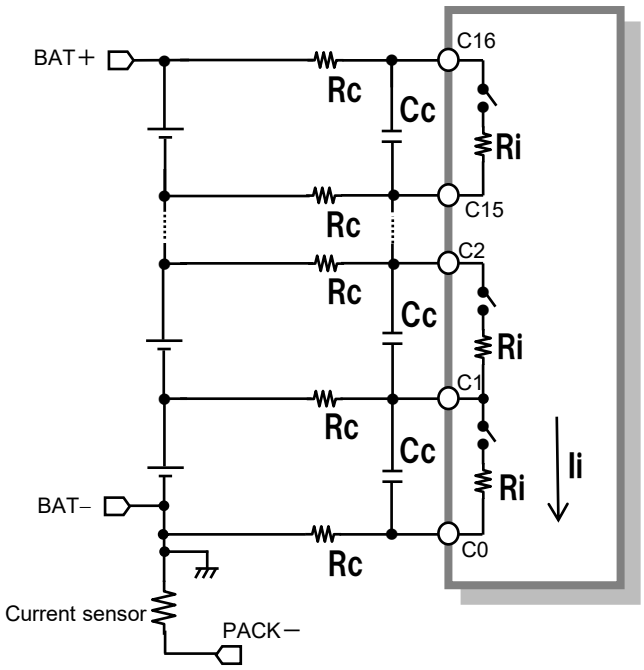


Fig. 2.2.1 Parameter for internal cell balance

1) *Calculate Rc*

$$Ii = \frac{Vcell}{2Rc + Ri}$$

$Ii\ depends\ on\ the\ design\ target\ of\ your\ system$
$(Max(Ii) = 50mA)$

$Suppose\ Vcell = 4.2V\ \ Ii = 50\text{mA}$

$$Rc \geq \frac{1}{2} * \left(\frac{Vcell}{Ii} - Ri\right) = 32ohm$$

2) *Calculate Cc*

$$fc = \frac{1}{2\pi * 2Rc * Cc} \leq \frac{fs}{2}$$

$fc\ depends\ on\ the\ sampling\ time\ of\ our\ system$
$(MAX(fc) = \left(\frac{fs}{2}\right) = \frac{1}{50us*2} = 10kHz)$

$eg.\ when\ fs = 20kHz, Rc = 40ohm$

$$Cc \geq \frac{1}{fs * \pi * 2Rc} = 0.2\text{uF}$$

$Using\ 10 * Cc\ \ is\ recommended$

Chapter 2 Input RC and components setting for Cell Balance operation

2.3 NMOS for external cell balancing

When applying VBAT, high voltage may occur transiently between the external FET pins for cell balance because normally there is RC filter at VBAT line.

External Cell balance FET with high voltage tolerance is highly recommended to withstand this transient spike.

In case high voltage tolerance FET cannot be used in the system, user can consider to separate VBAT from C16 as shown in Fig.2.3.2.

Battery cells connection sequence is documented on chapter 5.

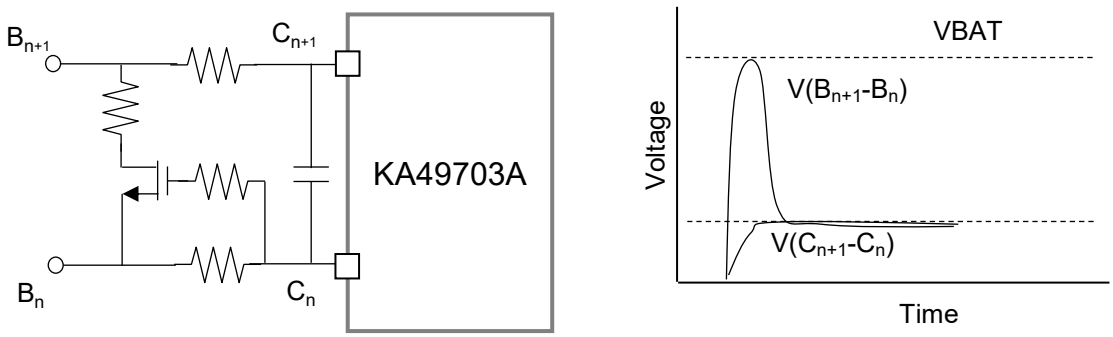


Fig. 2.3.1 Transient High Voltage

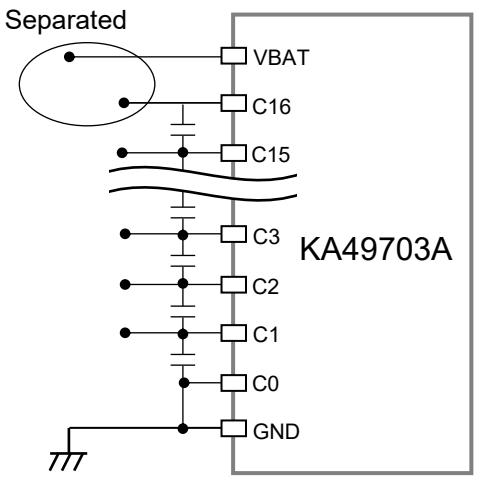


Fig. 2.3.2 Separated VBAT

Chapter 2 Input RC and components setting for Cell Balance operation

2.4 BJT for external cell balancing

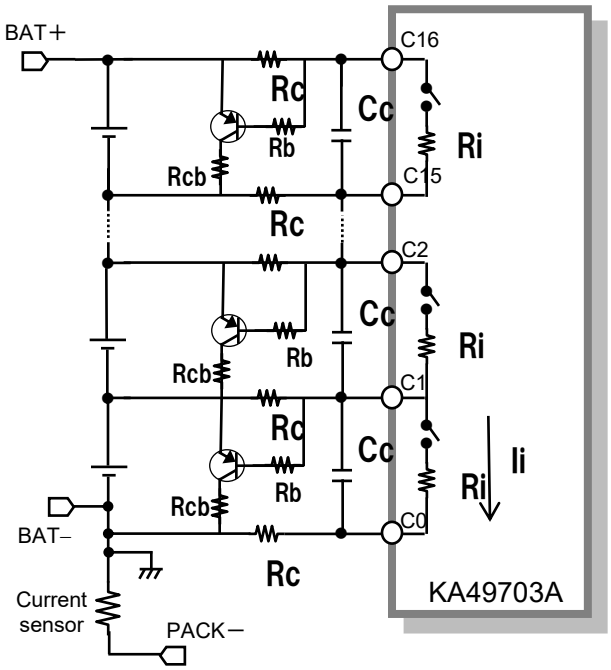


Fig. 2.4.1 Cell balance PNPc

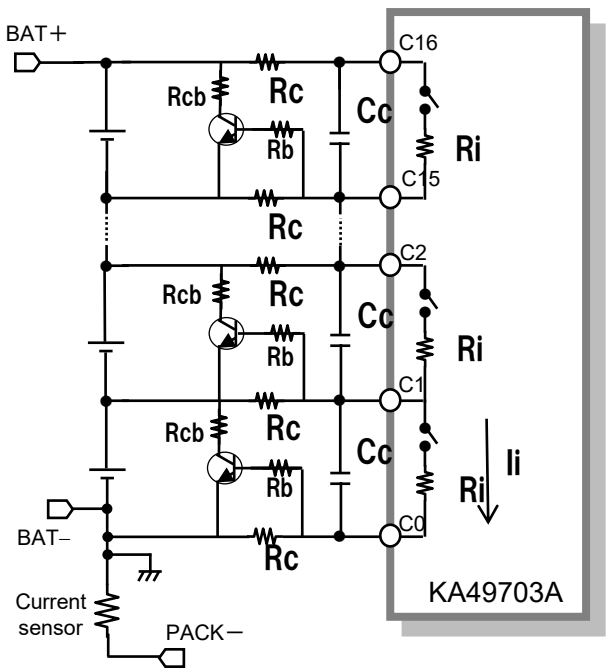


Fig. 2.4.2 Cell balance NPN

Example for parameter selection :

Rc=1kohm, Rcb =75ohm, Rb=100ohm

PNP BJT BC856 (Veb = 0.8V, Vce(sat)= -0.1V)

Icb = (Vcell - Vce(sat)) / Rcb = 48mA when Vcell = 3.7V

Chapter 2 Input RC and components setting for Cell Balance operation

2.5 Adjacent Cell Balance operation components setting

Figure2.5.1 below illustrates the circuit design for external cell balancing, with adjacent channels ON simultaneously. Recommended component values and BMIC registers setting can be found in chapter 5.1.3 of the KA49703A product standard.

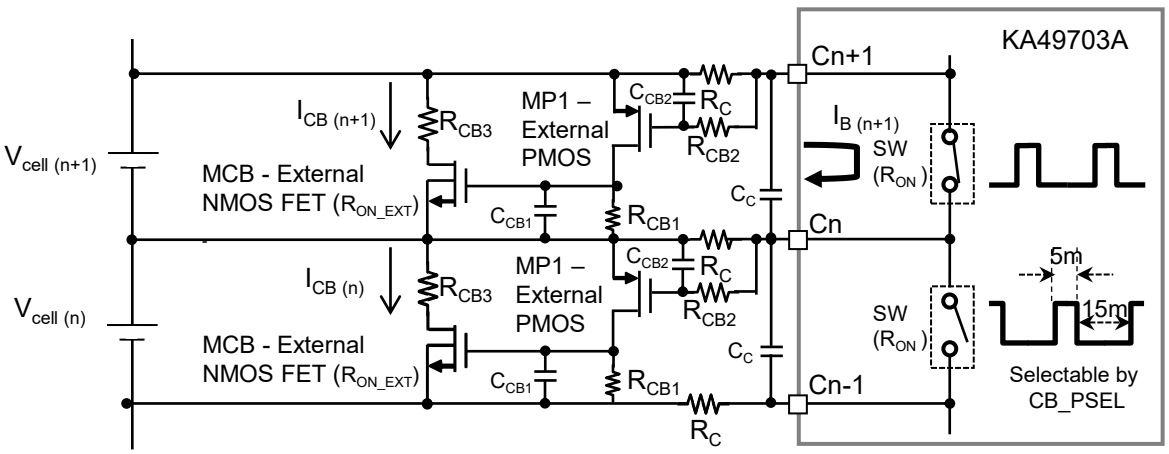


Fig.2.5.1 Circuit example with adjacent cell ON using external MOSFET

If the user wish to use MOSFETs different from the recommendation in the product standard, they can refer to Table 2.5.2 below for the components' selection characteristics.

Component	MOSFET Characteristic	Recommended Spec	Remark
MCB - NMOS	Vgs	>= 1V	- Vgs minimum 1V is necessary to ensure proper operation of this function - Vgs maximum depend on customer cell balance current requirement.
	Vds	>= 60V	- To cater for Hotplug
MP1 - PMOS	Vgs	Vcell/2	- Vgs maximum to ensure it still can turn on to drive 1MΩ resistor at Vcell = 2V

Table.2.5.2 External MOSFET Recommended Value

Chapter 2 Input RC and components setting for Cell Balance operation

2.6 Adjacent Cell Balance operation waveform

Table.2.6.1 below shows the recommended components for the adjacent cell balance operation with the correspondent cell balance ON refresh pulse period (CB_PSEL).

CB_PSEL [1:0] Setting	11 (50ms)	10 (25ms)	01 (0.5ms)	00 (5ms)	Remarks
Component	**Recommend Components Value or Part**				
C_C	1uF	0.47uF	0.1uF	0.1uF	CB_PSEL > 10*Rc*Cc
R_C	1kΩ	1kΩ	100Ω	1kΩ	
C_{CB1}	1uF	0.47uF	0.01uF	0.1uF	C_{CB1}*R_{CB1} >> 2*CB_PSEL to keep external CB switch turn on
R_{CB1}	1MΩ	1MΩ	1MΩ	1MΩ	
C_{CB2}	1nF	1nF	1nF	1nF	Recommend RC to filter noise
R_{CB2}	390kΩ	390kΩ	390Ω	390kΩ	
R_{CB3}	30Ω				Selected based on the cell balance current
MP1	Part number: DMG2305UXQ (Diodes Inc)				PMOS Switch to refresh C_{CB1} capacitor
MCB	Part number: Si2356DS (Vishay)				N Type Cell balance switch
CB_TPWM register	1 (160s)	1 (160s)	0 (16s)	0 (16s)	PWM operating period setting
OFF Time	1.6s	800ms	16ms	160ms	MCB off time

Table.2.6.1 Recommend BOM and register setting for circuit with adjacent cell balance ON

Timing of C2 pin balancing Timing of C3 pin balancing

Fig.2.6.2 Cell pins Voltage waveform with 5ms refresh pulse period

Chapter 2 Input RC and components setting for Cell Balance operation

2.6 Adjacent Cell Balance operation waveform

Figure 2.6.2 shows the voltage waveforms at cell pins C1 and C2, the gate-to-source voltage (Vgs) of the external NMOS, and the balancing current (I_{CB}) flowing through the cell pins during adjacent cell balancing. Figure 2.6.3 show the probe point in the circuit. Using the setting of 5ms refresh pulse period (CB_PSEL=00) and the recommended BOM in Table 2.6.1, the waveform indicates that the external NMOS gate voltage (Vgs) is refreshed periodically by the refresh pulse to stay higher than the gate-threshold voltage, enabling a continuous flow of balancing current between adjacent channels during the adjacent cell balancing.

Register Setting: CB_PSEL = 00 (5ms), CB_TPWM = 0 (16s), CB_SEL[0:1] = 00
(Cell 1 and Cell 2 CB ON), CB_ENADJ = 1 (Adjacent CB Enable)

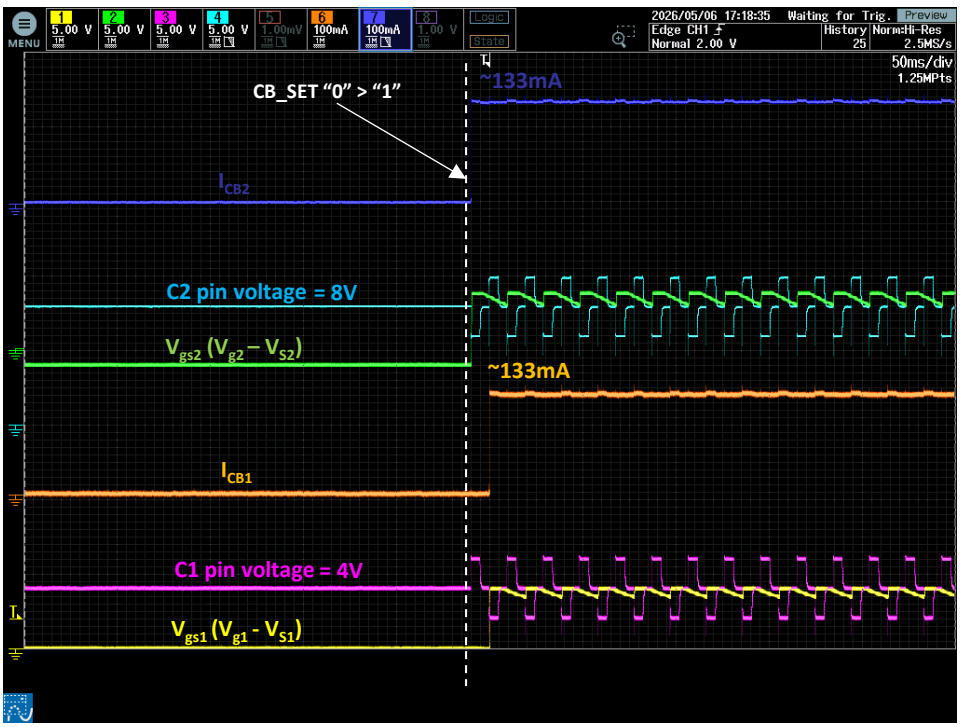


Fig. 2.6.2 Cell Balance Waveform for C1 and C2

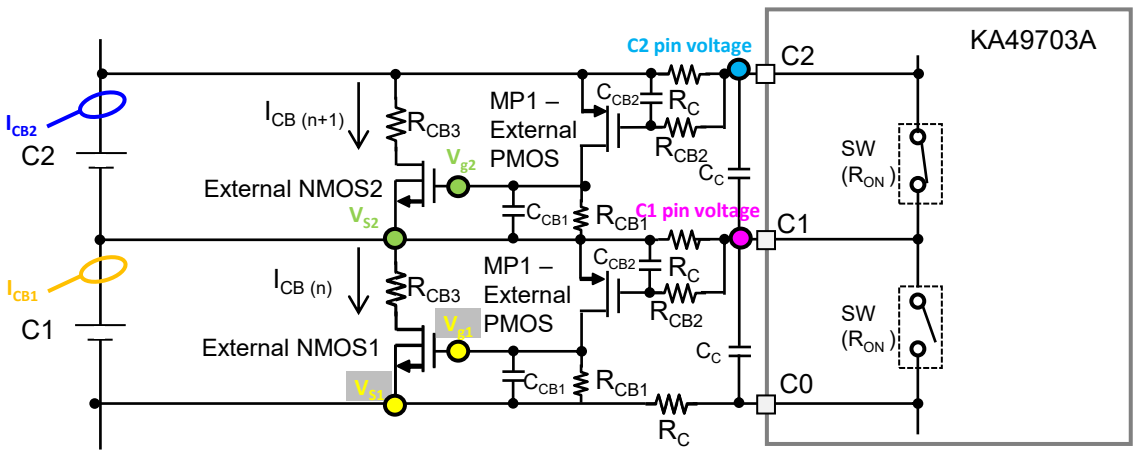


Fig. 2.6.3 Probe Point at Adjacent Cell Balance Circuit

Chapter 3 Regulators Components and setting

3.1 VDD50 RC and BJT components

VDD50 BJT and RC devices must be connected as shown in Fig. 3.1.1.

C_{REGB}, R_{REGB}, C_{VDD50}, R_{VDD50} should be selected according to the loop characteristic of the regulator design with the select NPN BJT. The recommended RC values with the accompany BJT devices are shown in Table. 3.1.2 below. These devices are to be used together with the recommended NPN BJT to ensure the best stability and load transient performance for VDD50 regulator. In case NPN BJT is changed from the recommended list, it is necessary to perform enough evaluation check and optimize the RC value again.

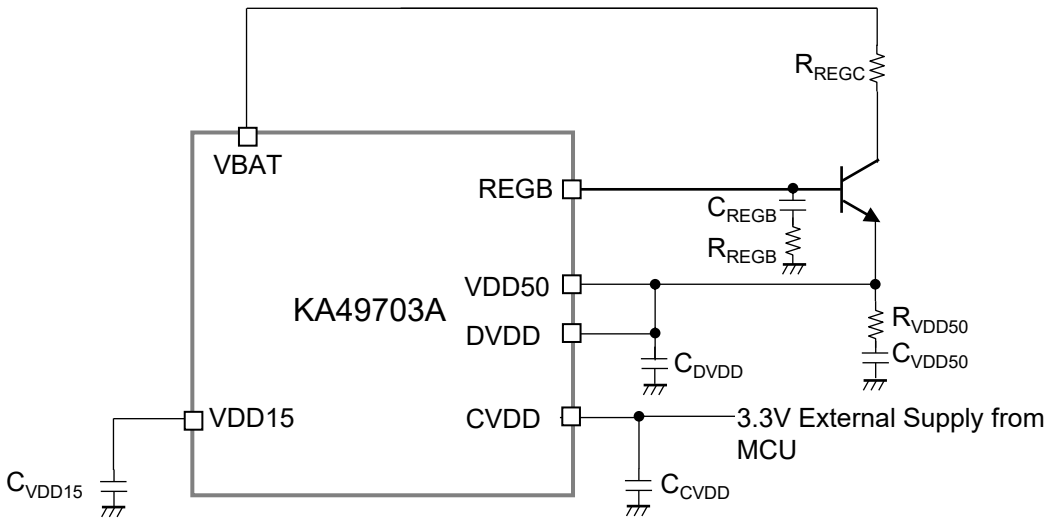


Fig. 3.1.1 VDD50 circuit

Component \ NPN	Recommended Component Value FZT458TA PZTA42T	Remark
C_{REGB}	0.1uF	<±50% for stability.
R_{REGB}	10kΩ	
C_{VDD50}	10uF	<±30% for stability.
R_{VDD50}	0.33Ω	
R_{REGC}	400Ω	Min VBAT > 30V for 50mA max load condition. Choose resistor with suitable power dissipation ability.
C_{CVDD}	1uF	Recommended for better transient response
C_{DVDD}	1uF	Recommended for better transient response
C_{VDD15}	4.7uF	

Table. 3.1.2 Recommended BOM for VDD50 regulator

Chapter 3 Regulators Components and setting

VDD50 BJT and RC devices must be connected as shown in Fig. 3.1.1.

When selecting the NPN BJT, it is recommended to consider the following key factor as listed in Table. 3.1.3 below. Recommended BJT are listed in Table. 3.1.2.

BJT Parameters	Minimum	Maximum	Notes.
DC current gain (h_{FE})	Depends on output current needed	Depends on stability of regulator.	$h_{FE} = I_C / I_B$ (I_B is base current from REGB pin. I_C is output collector current.) Do ensure to use NPN beta > 40
Continuous collector current (I_C)	Internal IC loading (2mA) + REGEXT loading needed (max 50mA)	Depend on NPN current rating as well as thermal performance	REGEXT can be used as power supply for external circuit. OCP of REGEXT is up to 100mA. Do ensure to use NPN beta > 40 to keep $I_{VDD55} > I_{REGEXT}$
Collector emitter voltage (V_{CEO})	> Charger input or >$VBAT_{max}$ with sufficient margin	--	Maximum battery level $VBAT_{max}$ or charger input voltage will be seen at V_{CE} of the NPN. It is necessary for selected NPN to be able to withstand this voltage applied to it with sufficient margin being considered.
Thermal	$Tj = (Pd \times \theta_{j-a}) + Ta$	--	(1) Tj ≦Tjmax BJT; (2) θ_{j-a}: Junction to ambient thermal Coefficient (It is recommended to have enough evaluation with the final PCB to determine actual θ_{j-a} and Tj of the NPN) (3) Ta=Ambient Temperature (4) Pd= ($VBAT_{max}$-5.0V) x I_{Cmax}

Table. 3.1.3 VDD50 BJT selection consideration

Chapter 3 Regulators Components and setting

3.2 CVDD settings

CVDD is a supply for the internal interface I/O pins GPIO1 to GPIO9. It can be connected to directly to VDD50 as shown in Fig. 3.2.1 for providing power for the interface I/O pins for internal usage.

For MCU that uses 3.3V supply, CVDD can be connected directly as shown in Fig.3.2.2. to the 3.3V supply of the MCU. It is recommended to have a capacitor placed close to CVDD pin to enhance transient response.

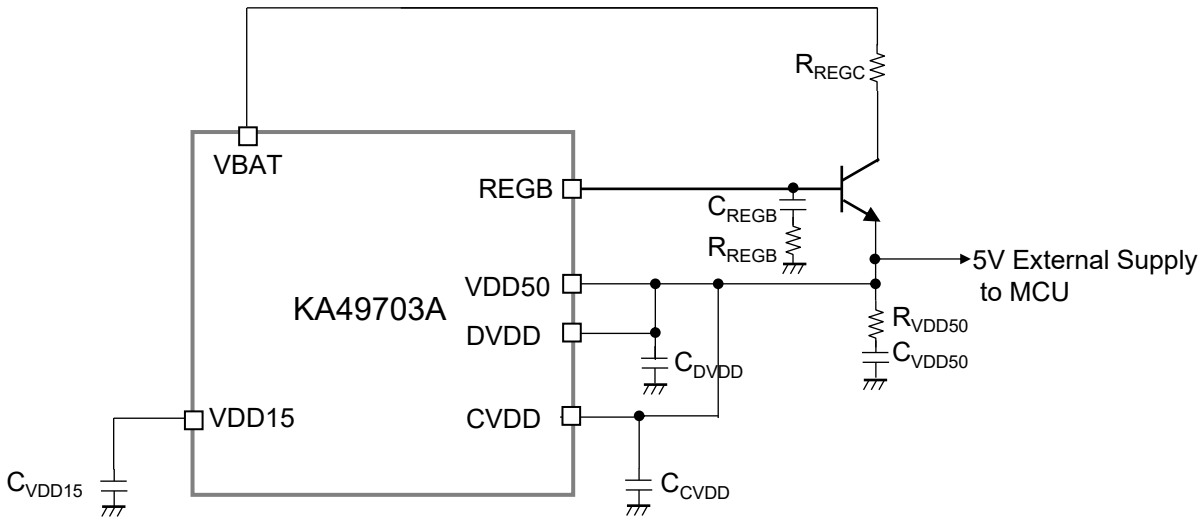


Fig. 3.2.1 CVDD connection using VDD50 supply

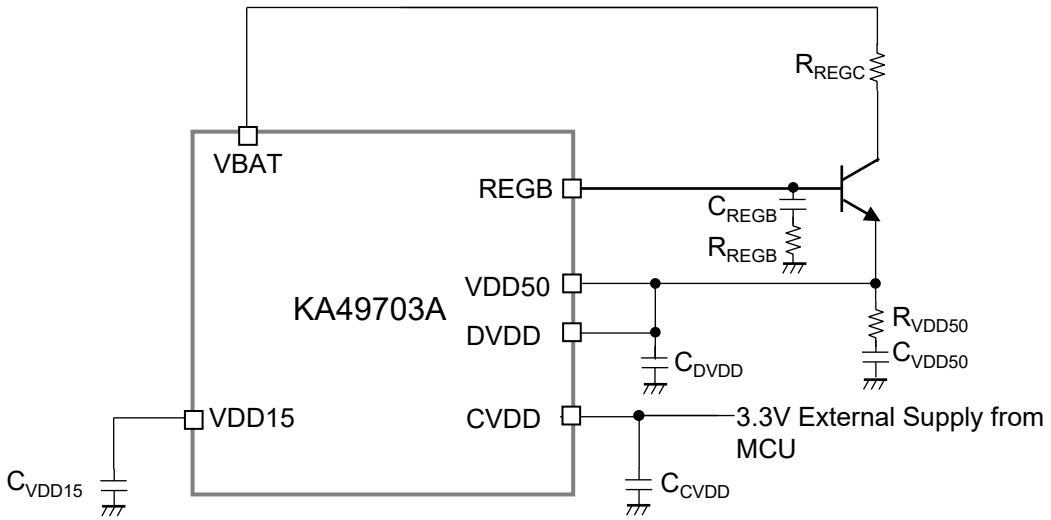


Fig. 3.2.2 CVDD connection using external supply

Chapter 4 Unused pins setting

4.1 Unused Cell Pins:

1) All unused Cell pins named 'NC' should be connected via resistor of the same input filter value to the cells. Refer to Fig 4.1.1
2) For lower cells count system, the unused battery cells pins (C3~C14) should be connected as shown in Fig 4.1.2 / 4.1.3 / 4.1.4
3) Fig.4.1.4 is an example for 4-cell solution, the cells can be added from lower to upper (C3,C4…) for the solution which need more cells.

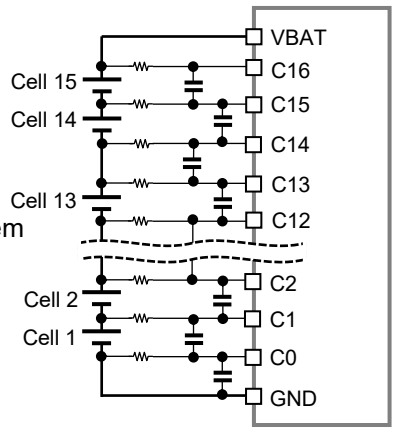


Fig. 4.1.1
Example of
15 Cell System

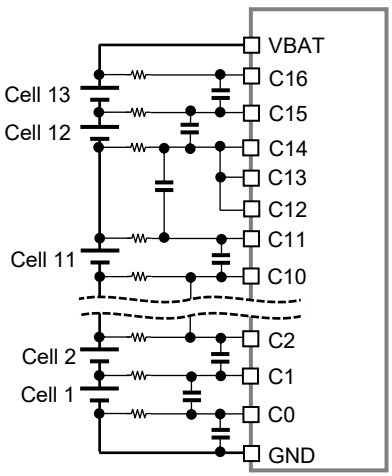


Fig. 4.1.2
Example of
13 Cell System

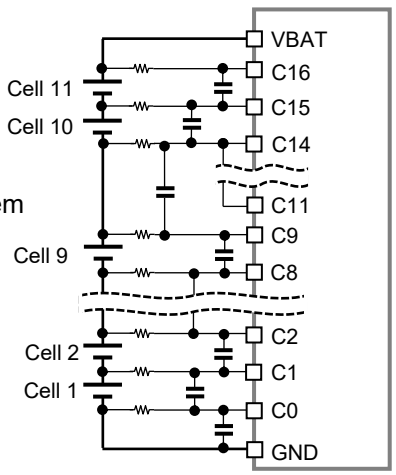


Fig. 4.1.3
Example of
11 Cell System

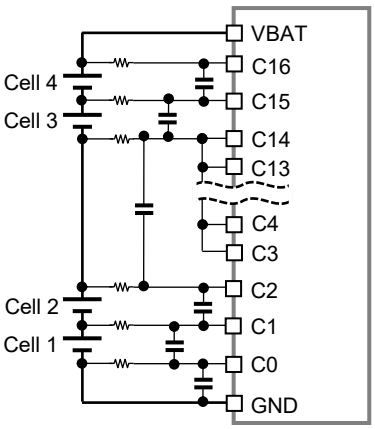


Fig. 4.1.4
Example of
4 Cell System

Chapter 4 Unused pins setting

4.2 Other unused pins:

Table.4.2.1 is a list for unused function pins and its recommended connection method when not used.

Function	Pin	Connection
Temperature	TMONIn (n=1~8)	Open
GPIO, Function and MCU Communication	GPIOn (n=1~9), TM_MX, ALM_I, ALM_O, SDO, SDI, SCL,SEN	Open
Function pin	WAKE	Ground
Daisy Chain Communication	DPL, DML, DPU, DMU	Open

Table. 4.2.1 Connection Example for unused function pins

Chapter 5 Battery Cell inputs connection sequence

5.1 Recommendation

Customer should strongly follow the below recommended Battery Cells connection sequence :

Connect the GND pin first, then followed by VBAT pin.

After that, connect lower cells in turn to upper cells.

GND → VBAT → Cell between C0-C1 → Cell between C1-C2 → Cell between…

5.2 Special case

If the recommended sequence can not be followed, but random connection or partial random connection sequence is required. Please use input resistors bigger than 100ohm for a fully random connection sequence.

For input resistors smaller than 100ohm, connect GND and VBAT first and than random connection for others cell voltage pin.

Note: Connection sequence for special case is verified by simulation with limited numbers of IC test, it seems no risks.

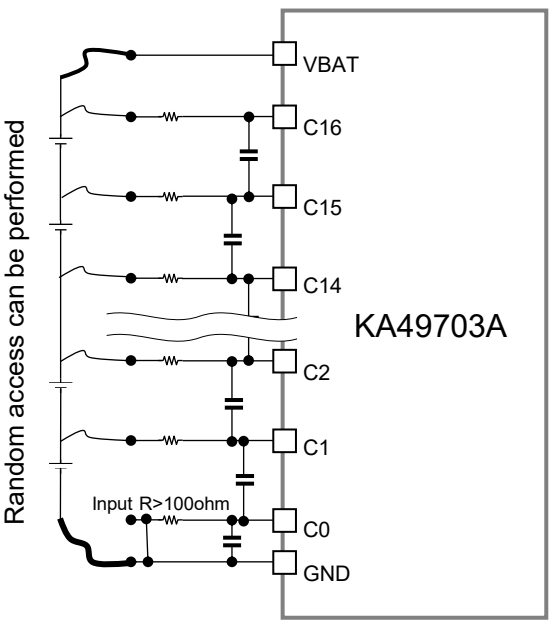


Fig. 5.2.1 Input Resistor bigger than 100ohm

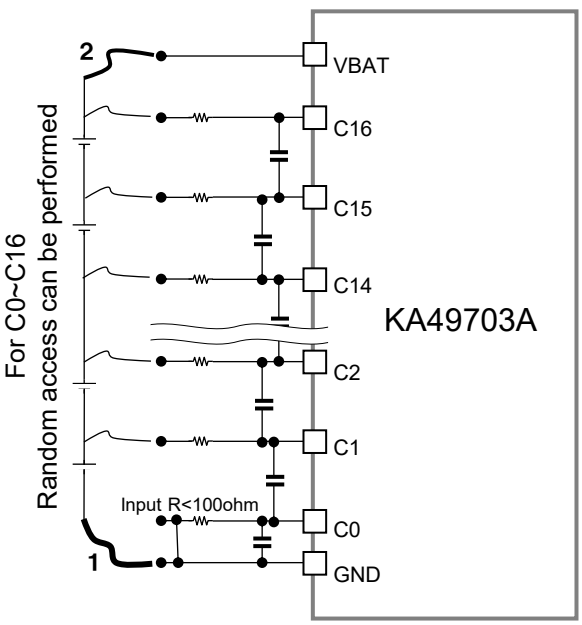


Fig. 5.2.2 Input Resistor smaller than 100ohm

Chapter 6 Daisy Chain Connection

6.1 Daisy Chain System Configuration

In a Daisy Chain system, KA49703 can function either as a master IC or as a slave IC and interact with other Nuvoton ICs. The figures below illustrate various Daisy Chain system setups utilizing different ICs.

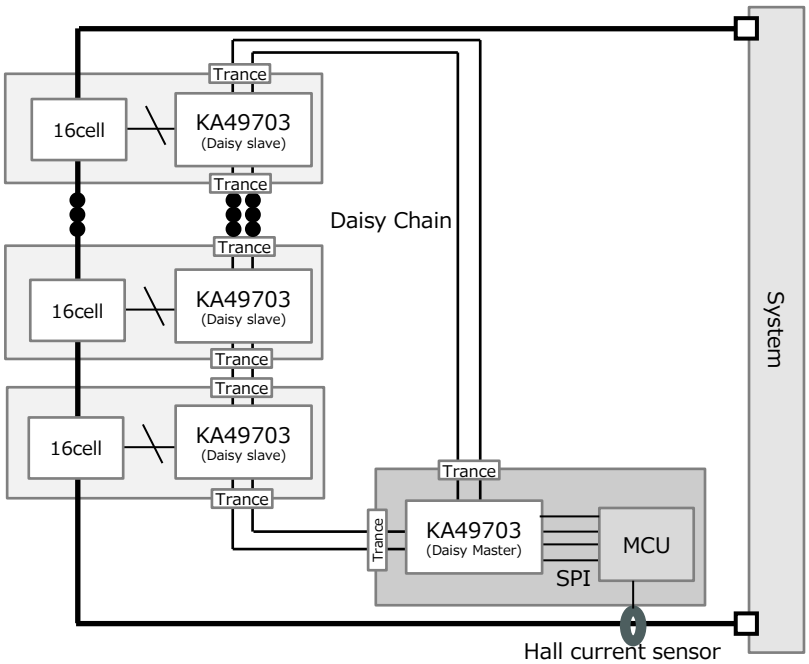


Fig. 6.1.1 Daisy System using KA49703 as Master IC

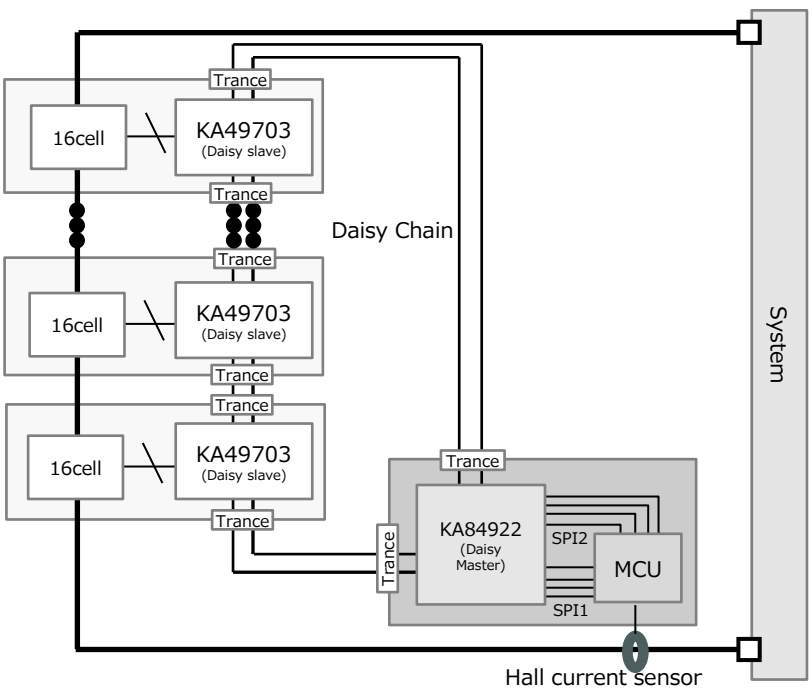


Fig. 6.1.2 Daisy System using KA84922* as Master IC

*KA84922 is a communication IC that converts 2 channels of SPI protocol to differential data stream.
More Information of this product can be found in Nuvoton Website, Link

Chapter 6 Daisy Chain Connection

6.1 Daisy Chain System Configuration

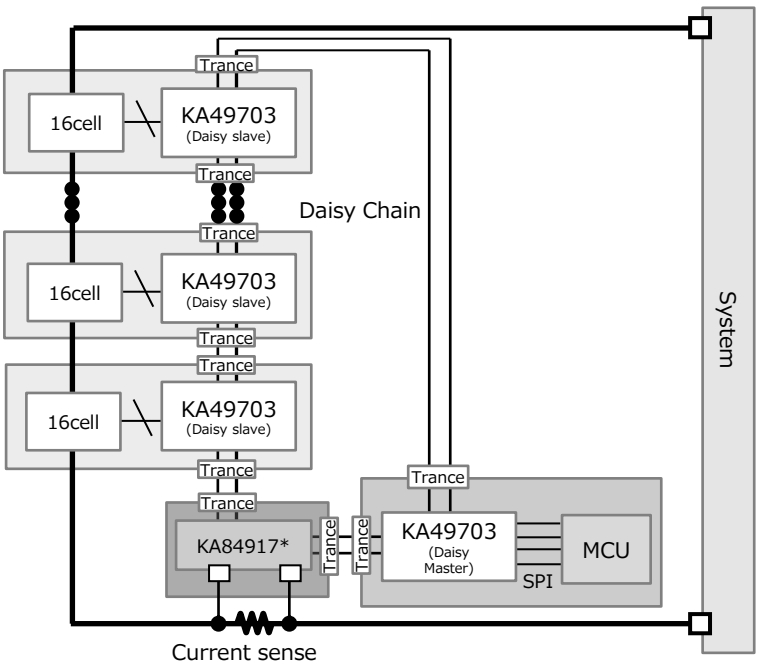


Fig. 6.1.3 Daisy System using KA49703 as Master IC with KA84917*

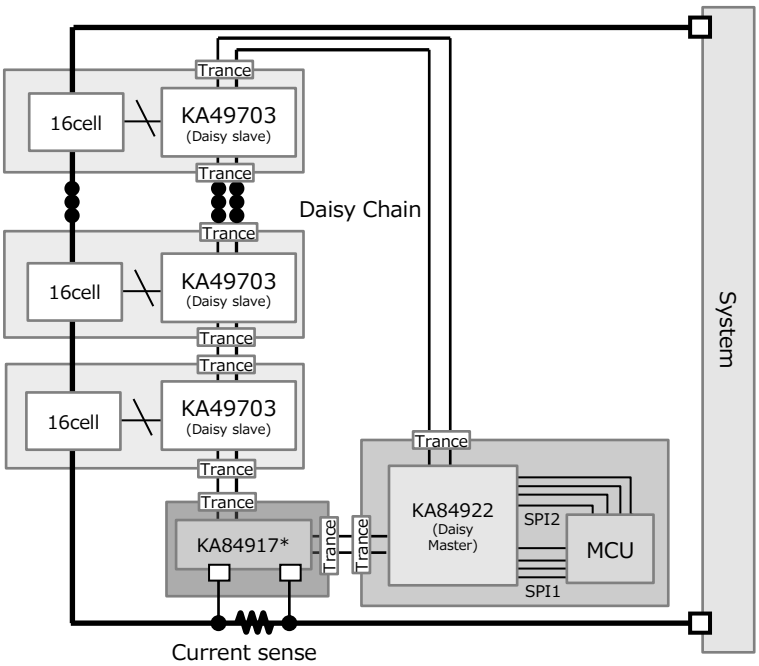


Fig. 6.1.4 Daisy System using KA84922 as Master IC with KA84917*

*KA84917 is a pack monitoring IC that measures current flowing through the battery pack. When using KA49703 as master IC, only register method (set SPIDIR_EN (address: 0x0C[14]) = “1”) can be used for direction control.
More Information of this product can be found in Nuvoton Website, Link

Chapter 6 Daisy Chain Connection

6.2 Daisy Chain connection between ICs using Transformer

The Daisy Chain connection between KA49703 and/or the Communication IC is connected through the DPU DPL and DMU DPL pins. The figure below illustrates the daisy chain setup using transformer method, along with the suggested transformer criteria and components to ensure effective communication.

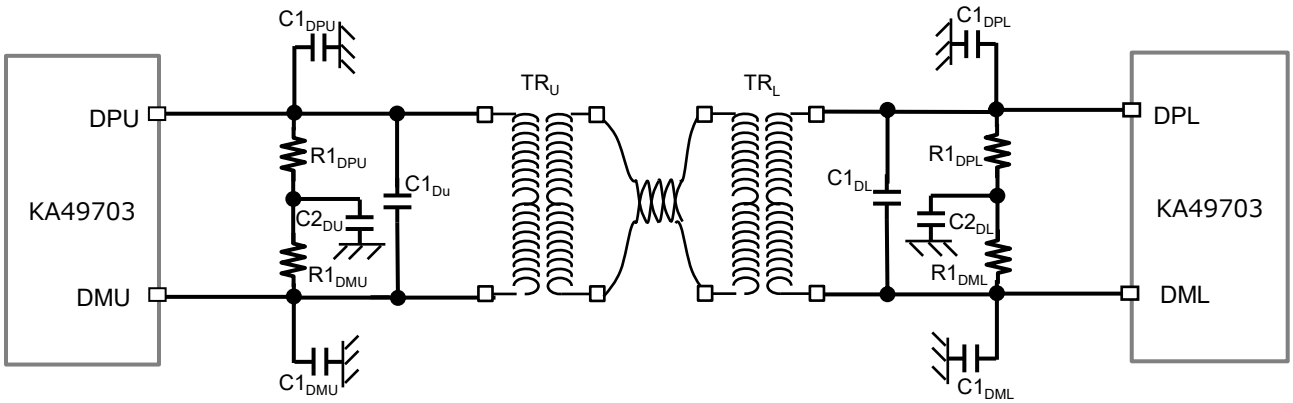


Fig. 6.2.1 Daisy Chain Connection using Transformer

Component	Recommended Component Value	Remark
$C1_{DPU}$, $C1_{DMU}$, $C1_{DPL}$, $C1_{DML}$	330pF	To reduce Daisy Wire noise
$R1_{DMU}$, $R1_{DPU}$, $R1_{DPL}$, $R1_{DML}$	51Ω	Refer to table 6.2.3 for selection characteristic
$C2_{DU}$, $C2_{DL}$,	1nF	Refer to table 6.2.3 for selection characteristic
$C1_{DU}$, $C1_{DL}$,	100pF	
TR_U, TR_L	Part number: TR34A25-1 (ESTON Tech)	Refer to table 6.2.3 for selection characteristic

Table 6.2.2 Recommended BOM for Daisy Chain Connection using Transformer

Transformer Characteristic	Recommended Spec
Inductance min	> 70uH
Leakage Inductance max	< 5.0uH
Stray Capacitance max	< 20pF
Interwinding Capacitance max	< 20pF
D.C.R max	< 1Ω
External RC – Terminal Resistor	51Ω +- 5% x 2
External RC – Resistor Centre Capacitor	1nF (50pF to 2nF)

Fig. 6.2.3 Transformer and RC components Characteristic

Chapter 6 Daisy Chain Connection

6.3 Daisy Chain connection between ICs using Capacitors

Alternatively, capacitors can be employed to establish a daisy chain connection between BMICs. Figure 6.3.1 below illustrates the daisy chain configuration utilizing a pair of capacitors, along with the recommended components in table 6.3.2.

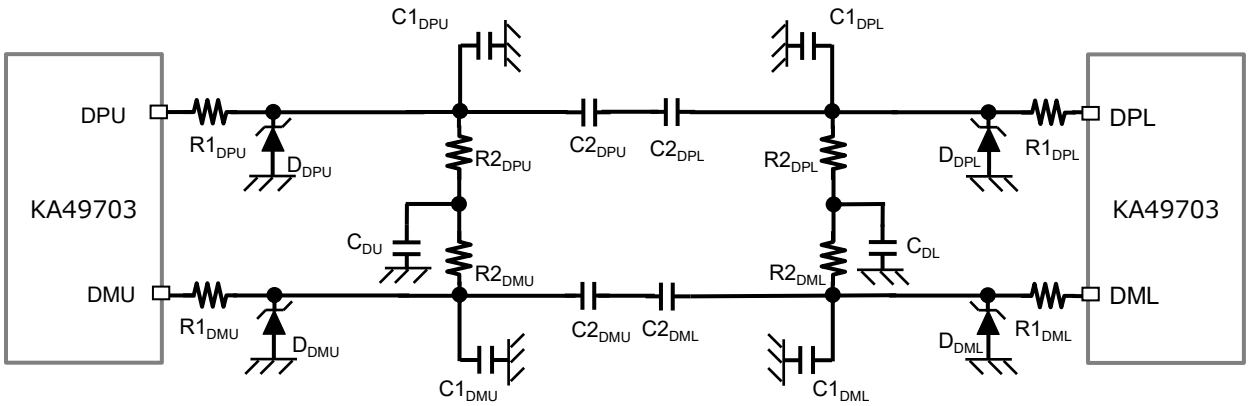


Fig. 6.3.1 Daisy Chain Connection using Capacitors Method

Component	Recommended Component Value	Remark
$R1_{DMU}$, $R1_{DPU}$, $R1_{DPL}$, $R1_{DML}$	10Ω	
D_{DPU}, D_{DMU}, D_{DPL}, D_{DML}	5.1V	Zener Diode
$C1_{DPU}$, $C1_{DMU}$, $C1_{DPL}$, $C1_{DML}$	330pF	Optional Component
$R2_{DMU}$, $R2_{DPU}$, $R2_{DPL}$, $R2_{DML}$	82Ω	
C_{DU}, C_{DL},	100nF	
$C2_{DPU}$, $C2_{DMU}$, $C2_{DPL}$, $C2_{DML}$	10nF	Filtering capacitor for high voltage communication line

Table 6.3.2 Recommended BOM for Daisy Chain Connection using Capacitors

Chapter 7 KA49703 as Communication IC Connection

7.1 Communication IC application

To setup KA49703 as communication IC, VDD50 and DVDD can be connected to the VBAT=5V directly as shown in Fig. 7.1.1.

For 5V MCU, CVDD can be connected directly to VBAT as shown in Fig. 7.1.1. For 3.3V MCU, CVDD can be connected as shown in Fig. 7.1.2 to the 3.3V supply of the MCU. It is recommended to have a capacitor placed close to CVDD pin to enhance transient response. Unused pins as depicted in Table 7.1.3 shall be left open.

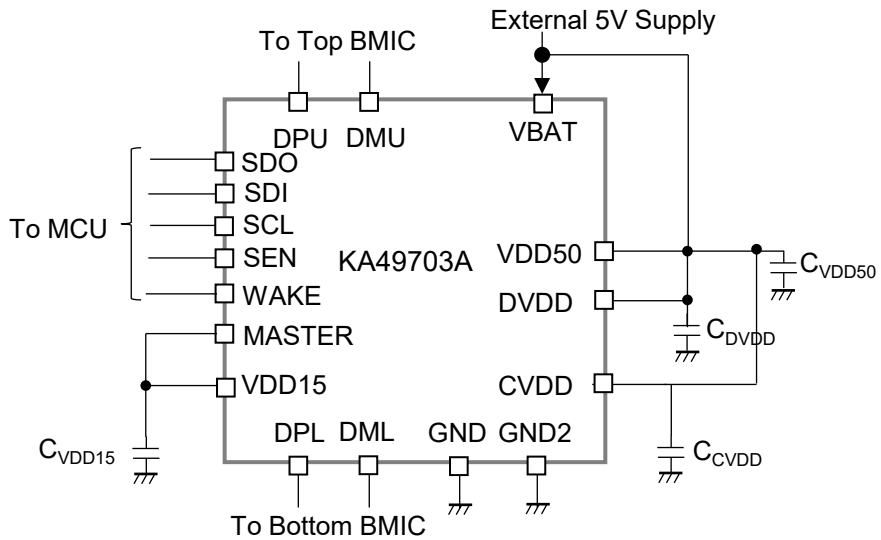


Fig. 7.1.1 Communication IC using VBAT=CVDD

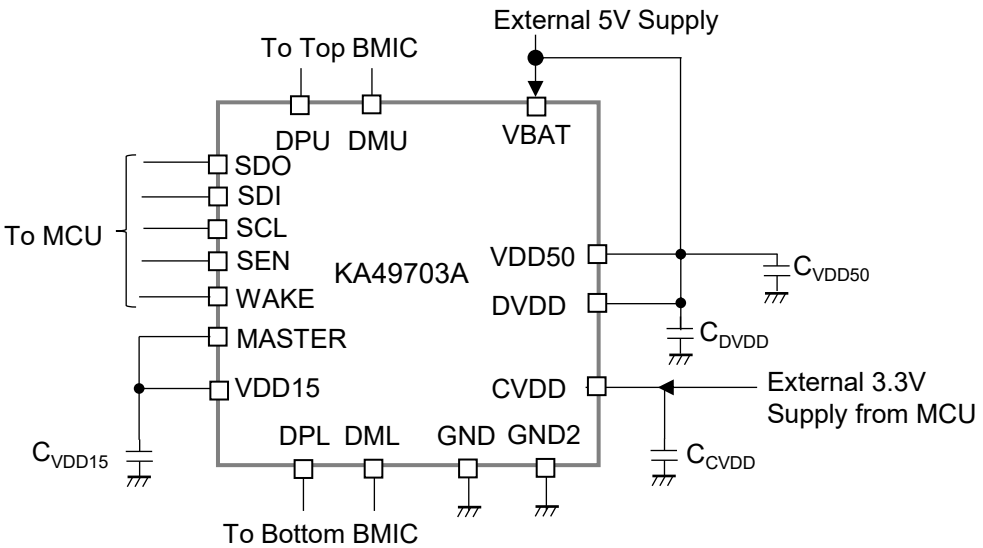


Fig. 7.1.2 Communication IC using CVDD=3.3V

Pin Number	Pin Name	Connection
Pin 12, Pin 14~30, Pin 32 ~39, Pin 40 ~44	REGB, C1 to C16, TMONI1 to TMONI8, GPIO1 to GPIO5	Open if unused

Table 7.1.3 Unused Pins Connection

Chapter 8 16-Channels TMONI using Multiplexer

The KA49703 features TMONI pins 1 ~ 8, which serve as temperature measurement inputs from NTC thermistors. For applications needing more than eight inputs, multiplexer circuit can be used to extend the TMONI voltage measurement capability to accommodate up to 16x NTC inputs. Figure 8.1 below illustrates how the TMONI pins connect with a multiplexer to enable measurement of 16 temperature inputs and the recommended components in table 8.2.

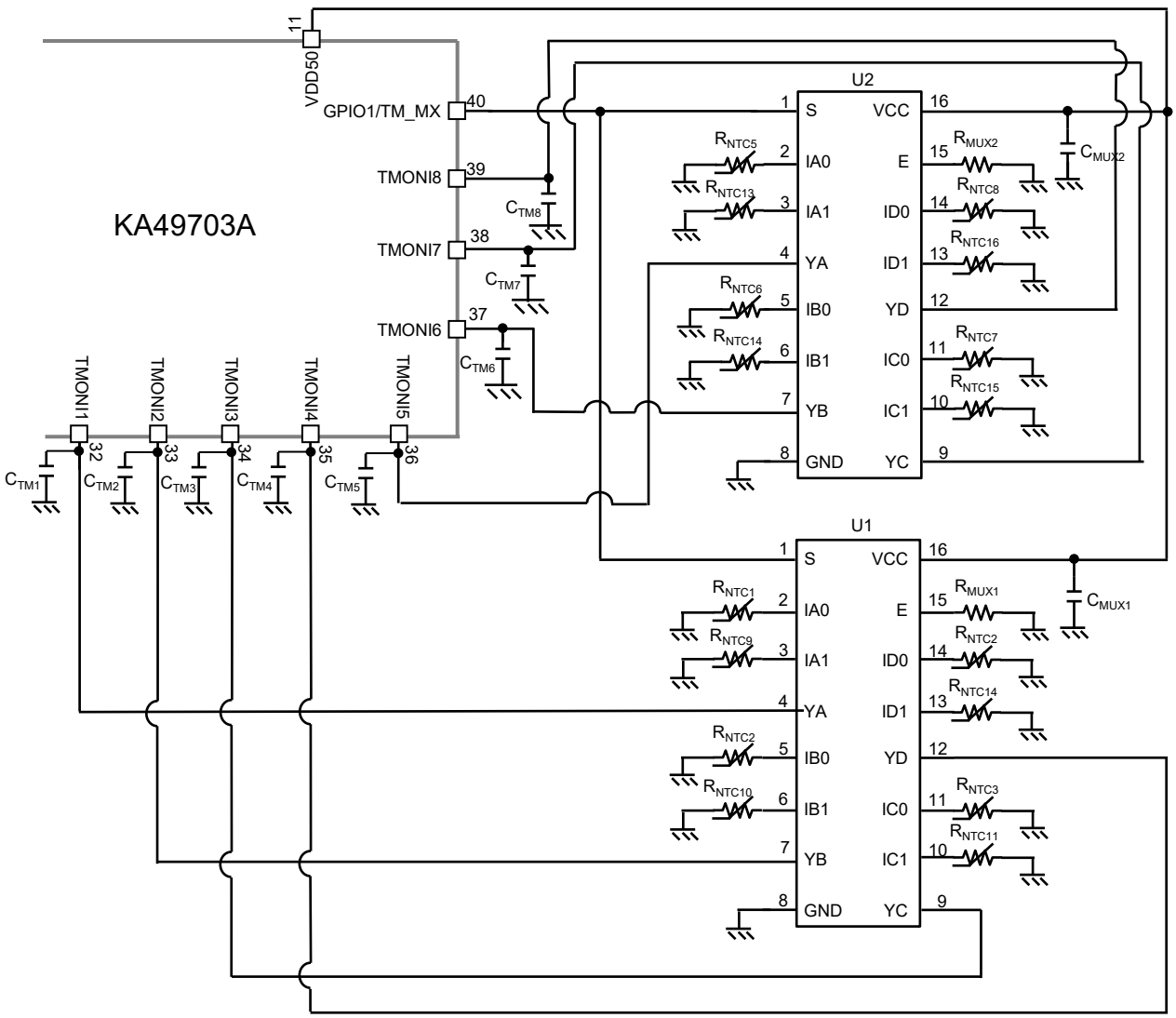


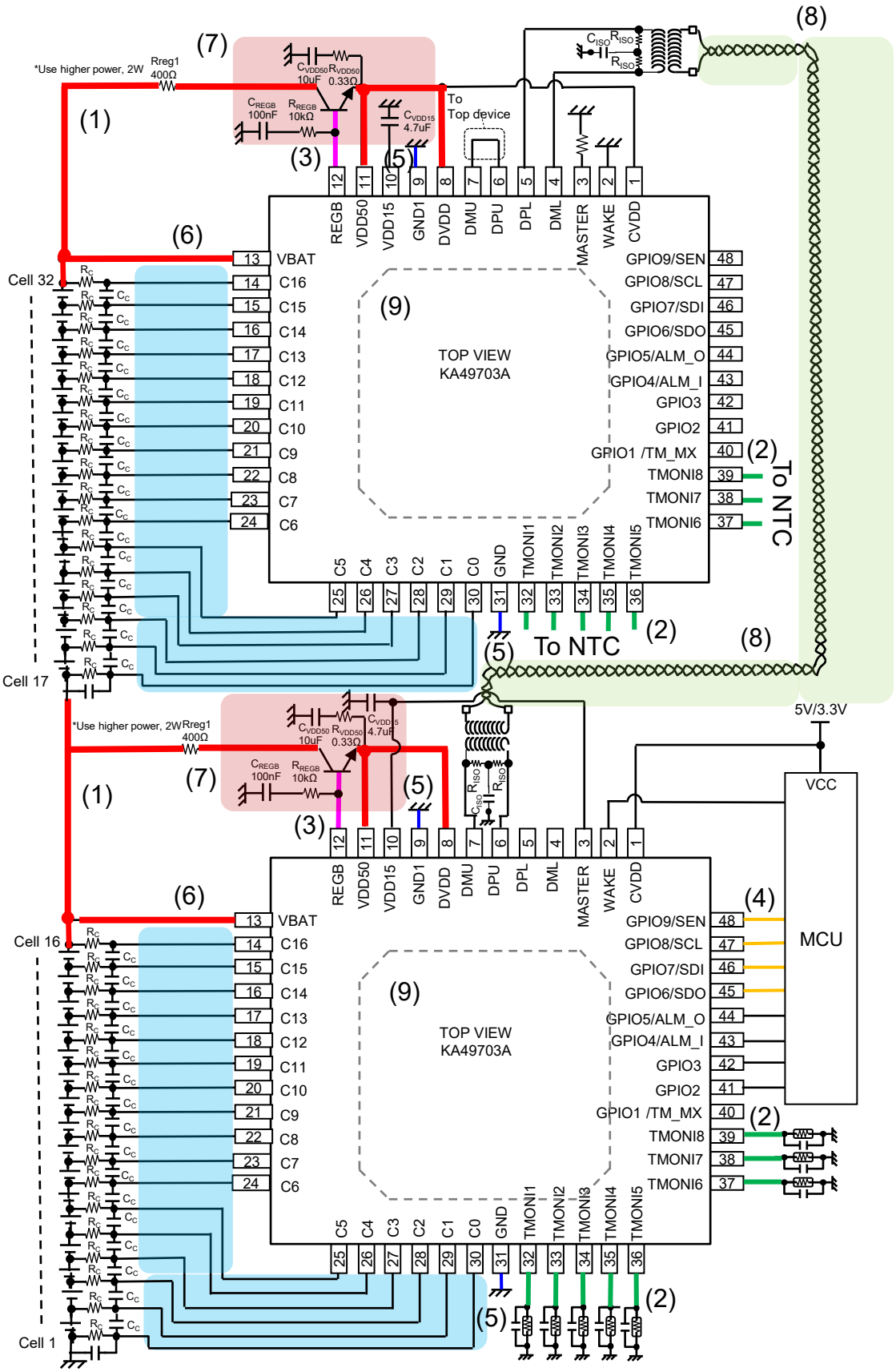
Figure. 8.1 16-Channels TMONI with Multiplexer Circuit

Chapter 8 16-Channels TMONI using Multiplexer

TMONI_PUTIM[1:0] (Addr: 0x14[15:15]) Setting	00 (190us)	01 (380us)	10 (570us)	11 (760us)	Remarks
Component	**Recommend Components Value or Part**				
C_{TM1}, C_{TM2}, C_{TM3}, C_{TM4}, C_{TM5}, C_{TM6}, C_{TM7}, C_{TM8}	1nF	TBD	TBD	TBD	- TMONI pin Filtering Capacitors - Set TMONI pullup time TMONI_PUTIM[1:0] according to Cap value
R_{NTC1}, R_{NTC2}, R_{NTC3}, R_{NTC4}, R_{NTC5}, R_{NTC6}, R_{NTC7}, R_{NTC8}	10kΩ				- NTC Temperature sensing resistors
C_{MUX1}, C_{MUX2}	0.1uF				
U1, U2	Part number: PI5C3257 (Diodes Inc)				- Quad 2:1 multiplexer

Table. 8.2 Recommended BOM TMONI with Multiplexer Circuit

Chapter 9 PCB Layout Guideline



Chapter 9 PCB Layout Guideline

(1) Wide line width to be drawn based on the desired Current.
(2) Away from signals lines. (*for TMONI/GPIO sharing pins, apply only when select TMONI function)
(3) Route lines as short as possible
(4) Insert capacitor if necessary, at communication lines according to your noise test
Draw all the SPI lines as short as possible and with same length to avoid propagation.
Draw all the SPI lines side by side and within the same layer.
Keep noisy lines and high voltage switching lines away from SPI lines.
(5) Connect all ground pins (GND) together and routed use copper plane under the IC
(6) Route these lines with the similar shape as much as possible since they are differential signals
(7) Devices to be placed close to IC pin
(8) Daisy Chain cable between BMIC, recommend twisted pair
(9) User can choose to float the bottom heat pad or connect it to GND plane for best heat dissipation

Important Notice

1. When using the IC for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this IC, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
3. This IC is intended to be used for general electronic equipment.
   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this IC may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
   (1) Space appliance (such as artificial satellite, and rocket)
   (2) Traffic control equipment (such as for automotive, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
   Our company shall not be held responsible for any damage incurred as a result of or in connection with the IC being used for any special application, unless our company agrees to the use of such special application.
   However, for the IC which we designate as products for automotive use, it is possible to be used for automotive.
4. This IC is neither designed nor intended for use in automotive applications or environments unless the IC is designated by our company to be used in automotive applications.
   Our company shall not be held responsible for any damage incurred by customers or any third party as a result of or in connection with the IC being used in automotive application, unless our company agrees to such application in this book.
5. Please use this IC in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Our company shall not be held responsible for any damage incurred as a result of our IC being used by our customers, not complying with the applicable laws and regulations.
6. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board),
   it might be damaged.
7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
   In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
9. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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Revision History

Revision number Rev 1.0

Date	Page	Item	Before	After
2025.10.23	—	—	—	First Version

Revision number Rev 1.1

Date	Page	Item	Before	After
2025.10.27	15	Add Note for KA84917 for support register mode only	"*KA84917 is a pack monitoring IC that measures current flowing through the battery pack. More Information of this product can be found in Nuvoton Website, Link"	"*KA84917 is a pack monitoring IC that measures current flowing through the battery pack. When using KA49703 as master IC, only register method (set SPIDIR_EN (address: 0x0C[14]) = "1") can be used for direction control. More Information of this product can be found in Nuvoton Website, Link"

Revision number Rev 1.2

Date	Page	Item	Before	After
2026.05.11	8, 9	Add Waveform for Adjacent Cell Balance	—	Add "2.6 Adjacent Cell Balance operation waveform" with recommend BOM, Adjacent CB waveform and explanation.